Fan Speed Controller with Linear or PWM Mode

Features

- **SMBus Interface**
- **Linear or PWM Mode Speed Control**
- **Open or Close Loop Fan Speed Control**
- **Supply Voltage Range 3V~5.5V**
- **ADD0 Pin to Select 3 Different SMBus Addresses**
- **SMBus Alert # for G763**
- **G763 has Built-in Inverter for Crystal Oscillator**
- **SOP-8/MSOP-8 for G762**
- **MSOP-10 for G763**

Applications

- **Notebook PC**
- **Industrial PC**
- **LAN Switch**
- **Servers**
- **Telecom equipment**
- **Industrial Control**

General Description

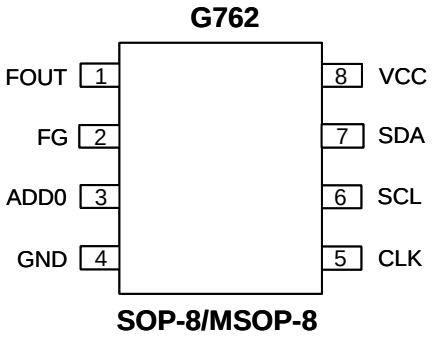
The G762/G763 is a single chip solution for fan speed control. It can be directly connected to the fan and performs close-loop or open-loop control. And there are two modes, PWM and linear, to drive the fan. It determined the current fan speed based on the fan rotation pulses and an externally supplied clock. The desired fan speed is programmed via the SMBus. The actual fan speed and fan status can be read via the SMBus. Short-circuit protection is implemented to prevent damages to the fan and the IC itself.

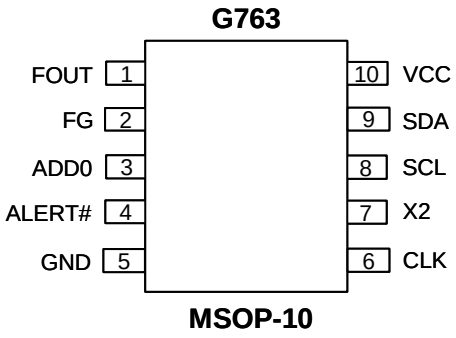
Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Pb free)
G762P11U	G762	-55°C to +125°C	SOP-8
G762P81U	G762	-55°C to +125°C	MSOP-8
G763P71U	G763	-55°C to +125°C	MSOP-10

Note: P1: SOP-8 P8: MSOP-8 P7:MSOP-10
1: Bonding Code
U: Tape & Reel

Pin Configuration





Absolute Maximum Ratings

VCC to GND . . . . . -0.3V to +6V
SCL, SDA, FG, ADD0, CLK . . . . . -0.3V to +6V
X2 ALERT# to GND
SDA ALERT# Current . . . . . .-1mA to +50mA
ESD Protection (human body model) 2000V
Continuous Power Dissipation (T_A = +70°C)
SOP(derate 8.30mW/°C above +70°C) 667mW
Operating Temperature Range . . . . . .-55°C to +125°C
Junction Temperature . . . . . .+150°C
Storage temperature Range . . . . . -65°C to +165°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = + 5V, T_A = 60°C, unless otherwise noted.)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Fan Controller					
FOUT Driver MOS On-resistance	SET_CNT=FFh, I_{FOUT}=5mA	---	1	---	Ω
FOUT Driver Current Limit	SET_CNT=FFh	---	1	---	A
FOUT Drive Current		---	500	---	mA
Fan Open Loop Output Differential Nonlinearity	Vcc=5V, I_{FAN}=Without Load	-1	---	1	LSB
Fan Open Loop Output Nonlinearity		-1	---	1	LSB
Fan Open Loop Output "code 1" Error		-2	---	2	LSB
Fan Open Loop Output Full Scale Error		-2	---	2	LSB
OUT PWM High-level Impedance	I_{FOUT}=5mA	---	1	---	Ω
OUT PWM Low-level Impedance	I_{FOUT}=-160µA	---	1.6k	---	Ω
CLK Pin Input Clock Frequency	CLK	---	32.768	---	kHz
FG Input Positive-going Threshold Voltage	V_{CC}=5V	---	2.3	---	V
FG Input Negative-going Threshold Voltage	V_{CC}=5V	---	750	---	mV
SMBus Interface					
Logic Input High Voltage	SMBCLK, SMBDATA; V_{CC} = 4.5V to 5.5V	---	2.4	---	V
Logic Input Low Voltage	SMBCLK, SMBDATA; V_{CC} = 4.5V to 5.5V	---	---	0.8	V
$\overline{\text{ALERT}}$ Logic Output Low Current	$\overline{\text{ALERT}}$, SMBDATA forced to 0.4V	6	---	---	mA
$\overline{\text{ALERT}}$ Output High Leakage Current	$\overline{\text{ALERT}}$ forced to 5.5V	---	1	---	µA
Logic Input Current	Logic inputs forced to V_{CC} or GND	-2	---	2	µA
SMBus Input Capacitance	SMBCLK, SMBDATA	---	5	---	pF
SMBus Clock Frequency		100	---	100k	Hz
SMBCLK Clock Low Time	t_{LOW} , 10% to 10% points	4.7	---	---	µs
SMBCLK Clock High Time	t_{HIGH} , 90% to 90% points	4	---	---	µs
SMBus Start-Condition Setup Time		4.7	-	---	µs
SMBus Repeated Start-Condition Setup Time	$t_{SU:STA}$, 90% to 90% points	500	---	---	µs
SMBus Start-Condition Hold Time	$t_{HD:STA}$, 10% of SMBDATA to 90% of SMBCLK	4	---	---	µs
SMBus Start-Condition Setup Time	$t_{SD:STO}$, 90% of SMBDATA to 10% of SMBDATA	4	---	---	µs
SMBus Data Valid to SMBCLK Rising- Edge Time	$t_{SU:DAT}$, 10% or 90% of SMBDATA to 10% of SMBCLK	800	---	---	µs
SMBus Data-Hold Time	$t_{HD:DAT}$	0	---	---	µs
SMBCLK Falling Edge to SMBus Data-Valid Time	Master clocking in data	---	---	1	µs

Note 1: Guaranteed but not 100% tested.
Note 2: Quantization error is not included in specifications for temperature accuracy.

Function Description

FAN Speed Measurement

The fan speed is measured by counting the number of the CLK pin period between the rising edges of two fan speed pulses on FG pin. In this way, we are actually measuring the period of the fan speed. This number is stored in FAN_ACT_CNT register. This count number, N, is used in the FAN control algorithm, thus, the desired fan speed should be programmed by reading the corresponding count number. The count number is given by:

N = (CLK × 30) / (RPM x P)

N : Count Number

RPM: FAN rotation speed, rotation per minute

P : FG pulses number per rotation of fan.

For CLK = 32768Hz, P = 2
⇒N = 491520 / rpm

For CLK = 16384Hz, P = 2
⇒N = 245762 / rpm

Some selected count numbers are shown below

Table 1. Count numbers for P=2

RPM	CLK=32768Hz	CLK=16384Hz
968	---	254
1935	254	127
2000	246	123
3000	164	82
4000	123	61
5000	98	49
6000	82	41
7000	70	35
8000	61	31
9000	55	27
10000	49	25
20000	25	12
30000	16	8

The formula of RPM versus FG_CLK_ID, FG_GEAR_MODE, FG_PLS_ID and SET_CNT (ACT_CNT) is

FG_CLK_ID: FG counting frequency

FG_GEAR_MODE: High speed fan setting factor

FG_PLS_ID: FG pulses number per revolution

Before setting the FAN_SET_CNT, make sure the FG_PLS_ID is fit the fan characteristic. Default FG_PLS_ID data bit is 0 for 2 pules/ revolution.

FAN_SET_CNT (FAN_ACT_CNT) = N: Count Number

If FG_GEAR_MODE = 0 (default)

FG_CLK_ID = 0 => N = 491520 / rpm

FG_CLK_ID = 1 => N = 245760 / rpm

FG_CLK_ID = 2 => N = 122880 / rpm

Some FAN_SET_CNT selected count number are listed below. (Table 2)

Table 2. RPM vs. Count Number at different FG_CLK_ID data bits

RPM	CLK_ID=00	CLK_ID=01	CLK_ID=10
500	N/A	N/A	246
1000	N/A	246	123
2000	246	123	61
3000	164	82	41
4000	123	61	31
5000	98	49	25
6000	82	41	20
7000	70	35	18
8000	61	31	15
9000	55	27	14
10000	49	25	12
20000	25	12	N/A
30000	16	N/A	N/A

FAN Gear-Mode

As to high rotation speed type fan, the FG counting number is smaller than lower speed one and the speed controlling accuracy is less than 2% when rotation speed is over 9500rpm(FG_CLK_ID=0). To increase the accuracy of the speed controlling we designed the Gear-Mode to solve this problem.

Table 3. RPM vs. Count Number at different FG_GEAR_MODE data bits

RPM	FG_GEAR _MODE =00	FG_GEAR _MODE =01	FG_GEAR _MODE =10
2000	246	N/A	N/A
3000	164	N/A	N/A
4000	123	246	N/A
5000	98	197	N/A
6000	82	164	N/A
7000	70	140	N/A
8000	61	123	246
9000	55	109	218
10000	49	98	197
20000	25	49	98
30000	16	32	66

If FG_CLK_ID = 0 (default)

FG_GEAR_MODE = 0 => N = 491520 / rpm

FG_GEAR_MODE = 1 => N = 983040 / rpm

FG_GEAR_MODE = 2 => N = 1966080 / rpm

Some FAN_SET_CNT selected count number are listed below. (Table 3.)

Fan Protection and Fan Fail Detections

There are fan fail detection circuits for the fan. Setting bit 7 of FAN_CMD1 registers high to activate the detection of fan failure. G762/63 defines fan failure as no transition on FG pin for about 0.7sec if FAN_SET_DAC is not set to 00h in open-loop control mode (or FAN_SET_CNT is not set to FFh in closed-loop control mode). Bit 7~ bit0 of status1 registers record the fan fail event. If fan failure events occur, ALERT pin goes low. To disable the fan-failure detection, set bit 7 of FAN_CMD1 register low.

In closed-loop control mode, if FAN actual RPM is 25% out of the programmed value for over 6 seconds (typical), bit in STATUS register is set low to indicate FAN out of control event. ALERT pin also goes low if this condition occurs. To disable the out of control detection, set bit 6 in FAN_CMD1 registers low.

FAN ACTUATION

FAN Driving Mode

G762/G763 drives the FOUT pin with linear mode or PWM mode by setting register FAN_CMD1 bit 5 0 or 1, respectively, Default is linear mode.

Linear Mode

In linear driving mode, the OUT pin voltage is determined by an internal DAC which voltage range is from 1/5VCC to VCC voltage with 500mA output current capacity.

$$\frac{V_{CC}}{5} + (\text{FANx\_SET\_DAC}) x \frac{1}{256} x \frac{4}{5} V_{CC}$$

The DAC voltage is 512 levels in close-loop control mode and 256 levels in open-loop control mode.

PWM Mode

In PWM driving mode, the FOUT pin will output PWM waveform with 25kHz and amplitude from GND to VCC voltage with sourcing impedance 1.6kΩ and sinking impedance 1Ω. The duty is 512 levels in close-loop control mode and 256 levels in open-loop control mode.

FAN Control Mode

By setting register 04h[4] to 1, it enters close-loop control mode. Write it with 0, it enters open-loop control mode. Defant value is 1, i.e., close-loop control mode.

Close-Loop Control

When it enters close-loop control mode, the driving voltage or duty is determined by the difference of register SET_CNT and ACT_CNT so that these two values become equal or 1 LSB error.

The SET_CNT is set by users. The ACT_CNT is obtained by counting FG rising edges using CLK pin frequency.

To stop the fan, program the fan speed register SET_CNT to 255.

Open-Loop Control

When it enters open-loop control mode, the driving voltage or duty is determined by FAN_SET_OUT register which makes a 2^8=256 levels of output voltage or output duty. The SET_CNT is set by users. The ACT_CNT is obtained by counting FG rising edges using CLK pin frequency.

In close-loop mode, ACT_CNT register is kept on updating the FG couting values. It won't be taken into account for output voltage or duty.

Fan Start up Voltage setting

To reduce the fan start up acoustic noise and fit the fan start up voltage G762/G763 provide a register can select 4 kind of start up voltage. User set FAN_CMD2 register data bit1 and bit0 to determine the start up voltage.(Table 4.)

Table 4. Fan Start Up Voltage Vs. Code

FAN_CMD2 bit 1,0	Start Up Voltage (VCC=5)
00	1.0V(Code=0)
01	1.5V(Code=32)
10	2.0V(Code=64)
11	2.5V(Code=96)

Controlling Fan at Lower Speed

For stably controlling fans at lower rotation speed, three schemes are recommended as below:

1.Use larger decoupling capacitors between FOUT and GND.

2.Shunt a capacitor of 1µF-2µF on FG pin to GND.

3.Use fans with open-collector FG outputs.

When controlling fans under lower rotation speed, the output voltage of FOUT would be too low for fan to generate recognizable FG signals.

Using decouple capacitors on FOUT and FG is to increase the SNR on FG pins. While using fans with open_collector FG outputs can thoroughly solve the problem, because the logic high level of FG would be fixed to 5V.

Over Temperature for Output Driver

G762/G763 provide over temperature protection function. When the chip temperature exceeds the high temperature threshold, 150°C typical, G762/3 will turn off the FOUT driving capacity.

SMBus Digital Interface

A standard SMBus 2-wire serial interface is used to read data or control the chip. The G762/G763 employs standard SMBus protocols: Write Byte, Read Byte, which are depicted in SMBus Timing chart.

SMBus Slave Address Selection

G762/G763 can be set to 3 different SMBus slave address by tieing ADD0 pin to VCC, GND or let it be floating. The selection is as Table. 5 describes

Table. 5 ADD0 Slave Address Selection

ADD0	SMBus Slave Address						
	A6	A5	A4	A3	A2	A1	A0
VCC	0	1	1	1	1	1	0
Floating	1	0	0	1	0	0	0
GND	1	0	0	1	0	0	1

The G762/G763 supports SMBus clock timeout function. When SMBCLK are held low for more than 30ms (typical) during an SMBus communication the G762/G763 will reinitiate its bus interface and be ready for a new transmission.

Alert Function and Status Registers

Any changing of bits of STATUS registers which indicate alarm, ALERT pin outputs low. The ALERT interrupt signal is latched and can only be cleared by reading the Alert Response address (Table 6). ALERT function can be disable by setting MASK bit in FAN_CMD2 registers. The ALERT pin is open-drain output. Connect a 10kΩ resister from ALERT pin to V_{CC}.

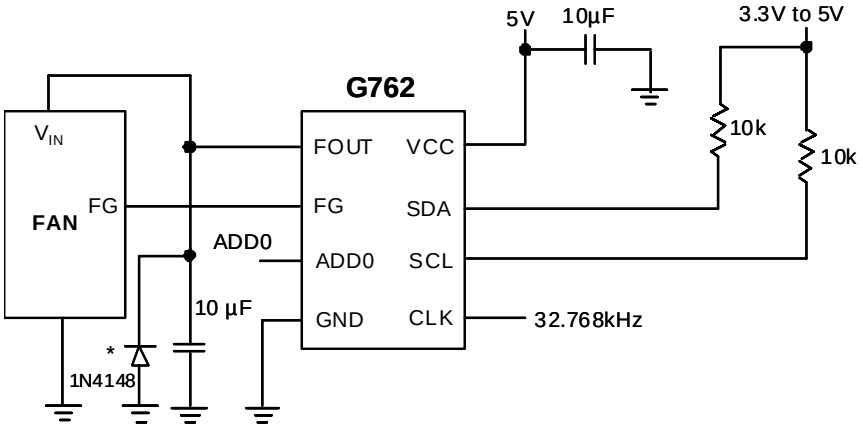
Table 6. Read Format for Alert Response Address (0001 100)

BIT	NAME
7(MSB)	ADD7
6	ADD6
5	ADD5
4	ADD4
3	ADD3
2	ADD2
1	ADD1
0(LSB)	1

Pin Description

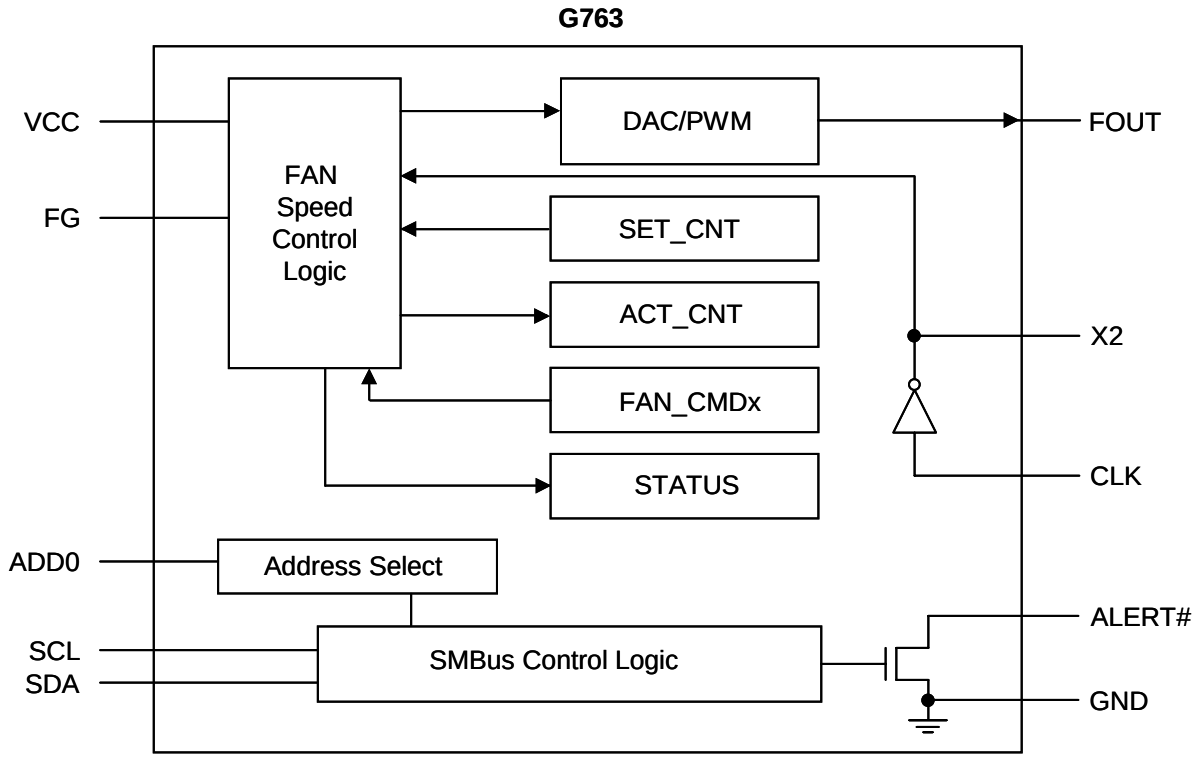
PIN		NAME	DIRECTION	FUNCTION
G762	G763			
SOP-8/MSOP-8	MSOP-10			
1	1	FOUT	Output	Output connected to fan driver circuit
2	2	FG	Input	Fan pulse input
3	3	ADD0	In/Out	SMBus slave address selection pin. VCC : 7'b0111_110 Float : 7'b1001_000 GND : 7'b1001_001
4	5	GND	Supply	Ground
5	6	CLK	Input	The input terminal of the built-in inverter for driving crystal.
6	8	SCL	Input	SMBus serial clock input
7	9	SDA	In/Out	SMBus serial data input/output, open drain
8	10	VCC	Supply	Supply Voltage
---	4	Alert#	Output	SMBus Alert output, open drain
---	7	X2	Output	The output terminal of the built-in inverter for driving crystal

Application Circuit



Diode 1N4148 is optional

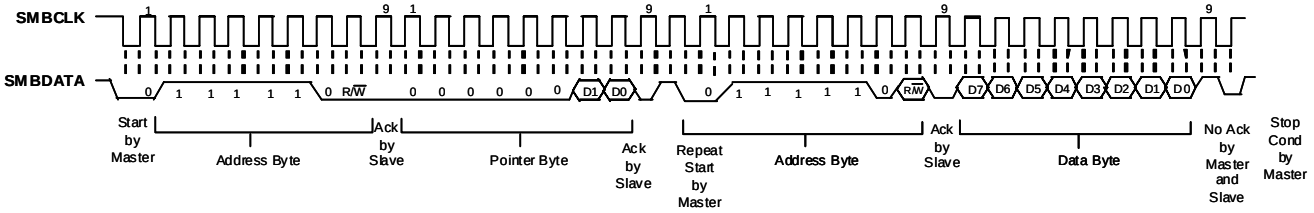
Block Diagram



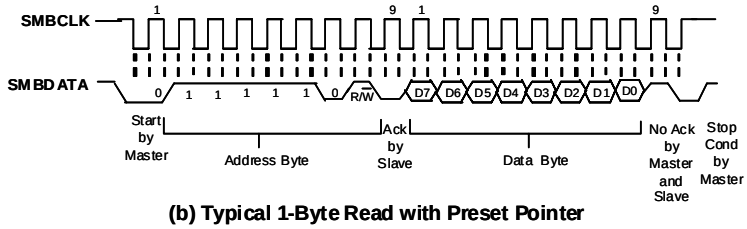
Registers Description

REGISTERS	COMMAND	POR	FUNCTION	R/W
FAN_SET_CNT	00h	11111111	Set FAN RPM in close loop control.	[7:0]R/W
FAN_ACT_CNT	01h	11111111	Read FAN RPM.	[7:0]R
STATUS	02h	xxxxxx01	Read status registers. bit 1: FAN_FAIL: FAN fail bit 0: FAN_ OOC#: FAN out of control	[1:0]R
FAN_SET_OUT	03h	00000000	Set FAN output voltage/PWM duty in open loop control.	[7:0]R/W
FAN_CMD1	04h	00010000	Read/Write FAN Configuration registers. **bit 7**: DET_FAN_FAIL . **bit 6**: DET_FAN_OOC **bit 5**: OUT_MODE 1:PWM , 0:DAC **bit 4**: FAN_MODE 1:close-loop 0:open-loop. ID of clock which to count FG. **bit 3**: FG_CLK_ID1, **bit 2**: FG_CLK_ID0, [FG_CLK_ID1, FG_CLK_ID0] 00: Divide fan clock by 1 01: Divide fan clock by 2 10: Divide fan clock by 4 11: Divide fan clock by 8 PWM output palarity **bit 1**: PWM_PLARITY,1:negative duty, 0:positive duty FG pulses count per revolution **bit 0**: FG_PLS_ID, 0:2 Pulses count per revolution. 1:4 Pulses count per revolution.	[7:0]R/W
FAN_CMD2	05h	xxx00001	Bit 4: Mask ALERT# for G763. Bit 3,2: FG_GEAR_MODE. 0,1,2 -> dT=Tfg/2,dT=Tfg,dT=2Tfg Bit 1,0: FAN_STARTV 0,1,2,3 -> 0,32,64,96 dac_code	[4:0]R/W

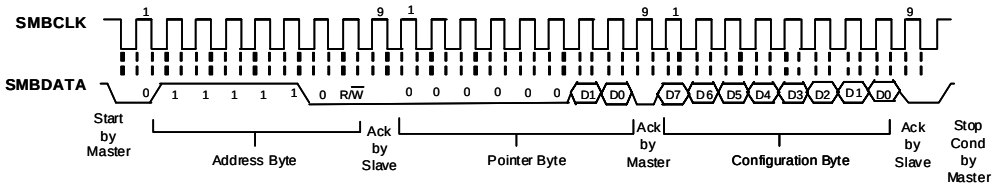
SMBus Timing



(a) Typical Pointer Set Followed by Immediate Read

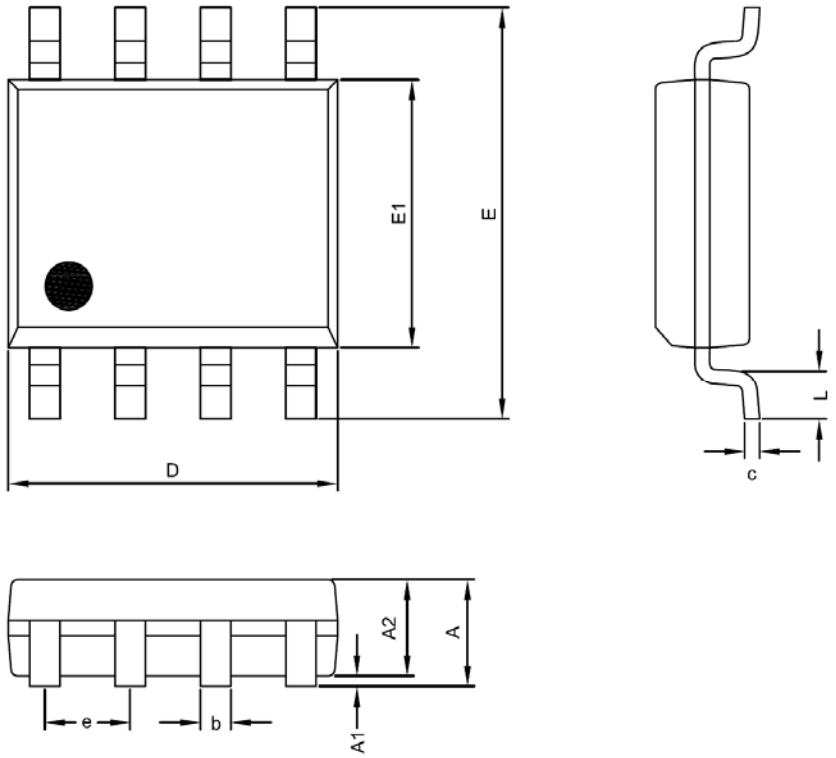


(b) Typical 1-Byte Read with Preset Pointer



(C) Register Write

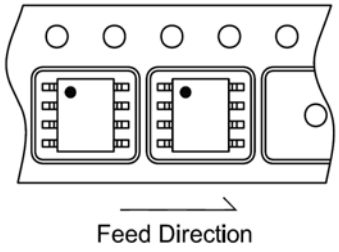
Package Information



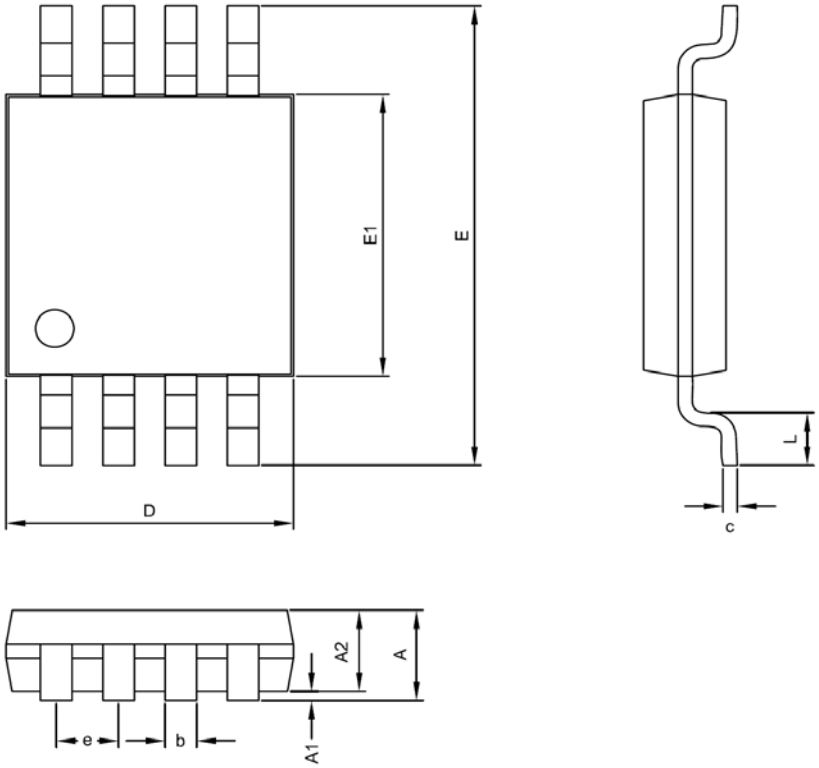
SOP-8 (P1) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.00	- - -	0.25	0.000	- - -	0.010
A2	1.15	1.35	1.50	0.045	0.053	0.059
D	4.80	4.90	5.00	0.189	0.192	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.153	0.157
c	0.19	0.23	0.27	0.007	0.009	0.011
b	0.33	0.43	0.53	0.013	0.017	0.021
e	1.27 BSC			0.050 BSC		
L	0.40	0.7	1.00	0.016	0.028	0.039

Taping Specification



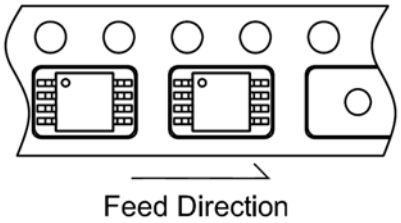
PACKAGE	Q'TY/REEL
SOP-8	2,500 ea



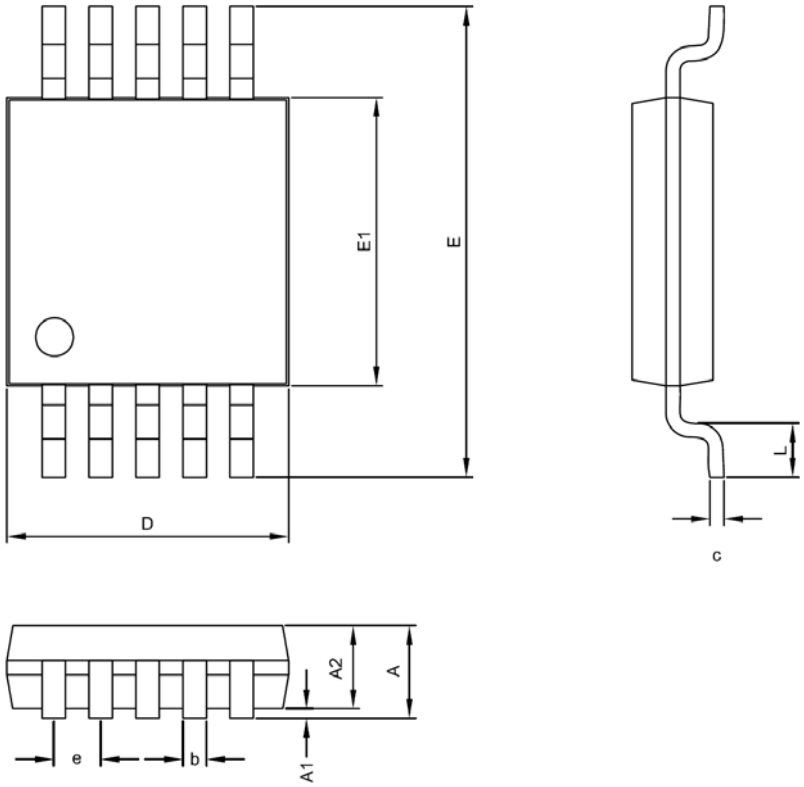
MSOP-8 (P8) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.95	1.10	0.032	0.037	0.043
A1	0.00	- - -	0.15	0.000	- - -	0.006
A2	0.76	0.86	0.96	0.030	0.034	0.038
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.13	0.15	0.23	0.005	0.006	0.009
b	0.28	0.30	0.38	0.011	0.012	0.015
e	0.65 BSC			0.026 BSC		
L	0.4	0.53	0.8	0.016	0.021	0.026

Taping Specification



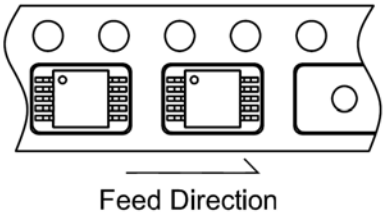
PACKAGE	Q'TY/REEL
MSOP-8	2,500 ea



MSOP-10 (P7) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.95	1.10	0.032	0.037	0.043
A1	0.00	- - -	0.15	0.000	- - -	0.006
A2	0.76	0.86	0.96	0.030	0.034	0.038
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.13	0.15	0.23	0.005	0.006	0.009
b	0.15	0.25	0.35	0.006	0.010	0.014
e	0.50 BSC			0.020 BSC		
L	0.40	0.53	0.66	0.016	0.021	0.026

Taping Specification



PACKAGE	Q'TY/REEL
MSOP-10	2,500 ea